ing n memory banks, and further comprising a first external clock having a first frequency and a second external clock having a second frequency equal to n times the first frequency, the method comprising the steps of:

(d) Transferring each of a multiplicity of system bus data signals having the second frequency to a memory bank data signal having the first frequency during a write operation, and transfer each of a multiplicity of memory bank data signals having the first frequency to a system data bus data signal having the second frequency during a read operation in a data MUX and latch subsystem

(e) Generating a memory bank strobe signal having the first frequency, and which is synchronized to the memory bank data signals with a 90 degree phase shift during the write operation, generating a system bus strobe signal having the second frequency which is synchronized to, and in phase with, the system bus data signals during the read operation in a strobe MUX and latch subsystem,:

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[c12] (f) generating a memory bank mask signal having the first frequency, and is synchronized to the memory bank data signals during the write operation in a mask MUX and latch subsystem.

[c13] 10. The method of claim 9, further comprising:

(a) increasing the duration of each data bit during both